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Claims

[c1] A method of forming a MOSFET semiconductor device, comprising:
providing a semiconductor substrate, said substrate comprising a buried insulating layer, a thin silicon layer overlying the buried insulating layer and a hard polish-stop layer overlying the thin silicon layer;
forming an isolation area surrounding and defining an active area of the MOSFET device;
selectively etching away the polish-stop layer to expose source/drain areas of the thin silicon layer;
implanting the exposed source/drain areas of the thin silicon layer to form source/drain junctions;
forming sidewall spacers surrounding the source/drain areas along vertical side walls of the isolation material and polish-stop layer between the source/drain areas;
depositing doped silicon to elevate the source/drain junctions;
forming source/drain silicide conductors on top of the elevated source/drain junctions;
forming protective caps over the source/drain silicide conductors;
removing the polish-stop layer between the source/drain

areas to form a gate opening;
forming a channel in the thin silicon layer;
forming a thin gate dielectric in the gate opening; and
forming a gate conductor in the gate opening over the gate dielectric.

[c2] A method according to claim 1, wherein:
the polish-stop layer is CVD diamond.

[c3] A method according to claim 1, wherein:
the buried insulation layer is oxide.

[c4] A method according to claim 1, wherein:
the substrate is a Silicon-on Insulator (SOI) substrate.

[c5] A method according to claim 1, wherein:
the isolation material is oxide.

[c6] A method according to claim 1, wherein:
the isolation oxide is formed by a Damascene process.

[c7] A method according to claim 1, wherein:
the gate conductor is polysilicon.

[c8] A method according to claim 1, further comprising:
forming metal wiring layers over the substrate; and
forming stud conductors to connect the source/drain silicide conductors and gate conductor to metal conductors in the metal wiring layers.

[c9] A method according to claim 1, wherein:
a Damascene process is employed to form the gate conductor.

[c10] A method according to claim 1, wherein:
the MOSFET semiconductor device is part of a CMOS circuit.

[c11] A method according to claim 1, wherein:
the MOSFET semiconductor device is part of an integrated circuit.

[c12] A MOSFET transistor comprising:
a semiconductor substrate, said substrate comprising a buried insulating layer, a thin silicon layer overlying the buried insulating layer and a hard polish-stop layer overlying the buried insulating layer;
STI (shallow trench isolation) completely surrounding and defining an active area (AA) of the MOSFET transistor and isolating the MOSFET transistor from other devices formed on the substrate
a channel and source/drain junctions defined in the thin silicon layer within the active area.

[c13] A MOSFET transistor according to claim 12, wherein:
a top surface of the STI is coplanar with a top surface of a gate conductor overlying the channel.

[c14] A MOSFET transistor according to claim 12, wherein:
a top surface of the STI is coplanar with a top surface of a gate conductor overlying the channel.

[c15] A MOSFET transistor according to claim 14, further comprising:
A "U" shaped gate dielectric formed between the gate and the sidewall spacers and channel.

[c16] A MOSFET transistor according to claim 14, wherein:
the gate conductor is polysilicon.

[c17] A MOSFET transistor according to claim 12, wherein:
the polish-stop layer is CVD diamond. A MOSFET transistor according to claim 12, wherein: the MOSFET transistor is part of an integrated circuit device.

[c18] A method of forming a MOSFET semiconductor device, comprising:
providing a SOI substrate, said substrate comprising a buried oxide layer, a thin silicon layer overlying the buried oxide layer and a CVD diamond polish-stop layer overlying the thin silicon layer;
forming an isolation trench surrounding and defining an active area of the MOSFET device, said trench extending downward through the hard polish-stop layer and thin silicon layer to the buried oxide layer;

filling the isolation trench with via a Damascene CVD oxide deposition process;
using an oxygen plasma etching process to selectively etch away the polish-stop layer to expose source/drain areas of the thin silicon layer, leaving behind a sacrificial dummy gate structure overlying a channel area of the thin silicon layer;
using an ion implantation process to dope the exposed source/drain areas of the thin silicon layer to form source/drain junctions;
forming sidewall spacers surrounding the source/drain areas along vertical side walls of the isolation material and dummy gate structure;
forming elevated source/drain junctions by employing a Damascene process to elevate the source drain junctions to a level flush with a top surface of the polish-stop layer followed by a controlled etching process to recess the elevated source drain junctions back to a suitable depth;
employing a silicidation process to form silicide atop the elevated source/drain junctions;
forming protective caps over the source/drain silicide conductors;
using a selective oxygen plasma etching process to removing the sacrificial dummy gate to form a gate opening;
ion implanting the channel area of the thin silicon layer

to form a channel;

forming a thin gate dielectric in the gate opening;

forming a gate conductor in the gate opening over the gate dielectric and planarizing such that a top surface of the gate conductor, tops of the sidewall spacers and a top surface of the STI are all coplanar;

forming first and second-level metal interconnect layers and connecting the source/drain silicide conductors and gate conductor to respective metal conductors in the interconnect layer via conductive studs.